In the Claims:

Claims 1-22 (Cancelled).

23. (Currently Amended) A MOSFET comprising:

a semiconductor layer having a trench therein;

a gate conducting layer in a lower portion of the trench;

a dielectric layer in an upper portion of the trench ~~and extending outwardly from said semiconductor layer, the outwardly extending dielectric layer having sidewalls aligned with sidewalls of the trench~~;

source regions adjacent said dielectric layer ~~the outwardly extending dielectric layer~~; and

source/body contact regions laterally spaced apart from said gate conducting layer and non-interruptibly contacting said source ~~regions~~ regions;

said dielectric layer extending outwardly from said semiconductor layer, said source regions and said source/body contact regions, and said outwardly extending dielectric layer having sidewalls aligned with sidewalls of the trench.

24. (Previously Amended) A MOSFET according to Claim 23, further comprising a source electrode on said source regions and on said dielectric layer.

25. (Original) A MOSFET according to Claim 24, further comprising at least one conductive via between said source electrode and said source/body contact regions.

26. (Original) A MOSFET according to Claim 23,

wherein a portion of said source regions include a recess over said source/body contact regions.

27. (Original) A MOSFET according to Claim 23, wherein a portion of said source regions include an opening exposing said source/body contact regions; and further comprising a source electrode on said source regions, on said dielectric layer, and on said source/body contact regions.

28. (Original) A MOSFET according to Claim 23, wherein said outwardly extending dielectric layer extends from said source regions equal to or less than about 1 micron.

29. (Original) A MOSFET according to Claim 23, wherein the gate is recessed in the trench within a range of about 0.2 to 0.8 microns from an opening thereof.

30. (Original) A MOSFET according to Claim 23, wherein said source/body contact regions are recessed within said semiconductor layer adjacent said source regions.

31. (Original) A MOSFET according to Claim 30, wherein an upper surface of the recess is equal to or less than a depth of about 1 micron from a surface of the semiconductor layer.

32. (Currently Amended) A MOSFET comprising:
a semiconductor layer having a trench therein;
a gate dielectric layer lining the trench;
a gate conducting layer in a lower portion of the

trench;

a dielectric layer in an upper portion of the trench ~~and extending outwardly from said semiconductor layer, the outwardly extending dielectric layer having sidewalls aligned with sidewalls of the trench~~;

source regions adjacent said dielectric layer ~~the outwardly extending dielectric layer~~;

source/body contact regions laterally spaced from said gate conducting layer and non-interruptibly contacting said source regions;

said dielectric layer extending outwardly from said semiconductor layer, said source regions and said source/body contact regions, and said outwardly extending dielectric layer having sidewalls aligned with sidewalls of the trench;

a source electrode on said source regions and on said dielectric layer; and

at least one conductive via between said source electrode and said source/body contact regions.

33. (Previously Added) A MOSFET according to Claim 32, wherein a portion of said source regions include a recess over said source/body contact regions.

34. (Previously Added) A MOSFET according to Claim 32, wherein said outwardly extending dielectric layer extends from said source regions equal to or less than about 1 micron.

35. (Previously Added) A MOSFET according to Claim 32, wherein said gate conducting layer is recessed in the trench within a range of about 0.2 to 0.8 microns from an

opening thereof.

36. (Currently Amended) A MOSFET comprising:

a semiconductor layer having a trench therein;

a gate dielectric layer lining the trench;

a gate conducting layer in a lower portion of the trench;

a dielectric layer in an upper portion of the trench and extending outwardly from said semiconductor layer, the outwardly extending dielectric layer having sidewalls aligned with sidewalls of the trench;

source regions adjacent said dielectric layer and including an opening therein; and

source/body contact regions laterally spaced from said gate conducting layer and non-interruptibly contacting said source regions, said source/body contact regions being exposed by the opening in said source ~~regions~~ regions;

said dielectric layer extending outwardly from said semiconductor layer, said source regions and said source/body contact regions, and said outwardly extending dielectric layer having sidewalls aligned with sidewalls of the trench.

37. (Previously Added) A MOSFET according to Claim 36, further comprising a source electrode on said source regions, on said dielectric layer, and on said source/body contact regions.

38. (Previously Added) A MOSFET according to Claim 36, wherein said outwardly extending dielectric layer extends from said source regions equal to or less than about 1 micron.

39. (Previously Added) A MOSFET according to Claim 36, wherein said gate conducting layer is recessed in the trench within a range of about 0.2 to 0.8 microns from an opening thereof.